Document control number:	<b>48</b> -00558
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# CGP-100/200 Graphics Processor Conversion Module

Logic Diagrams

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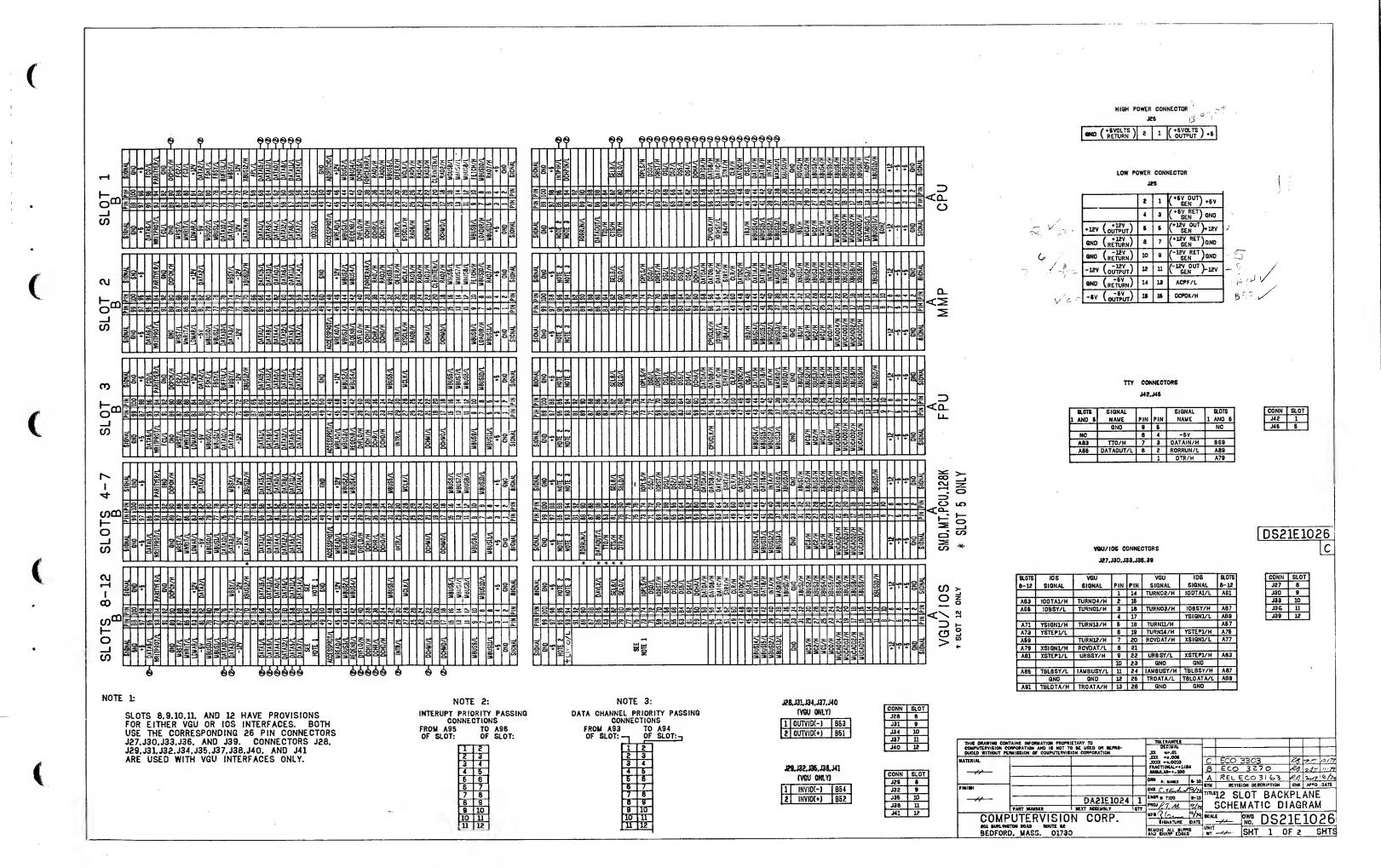
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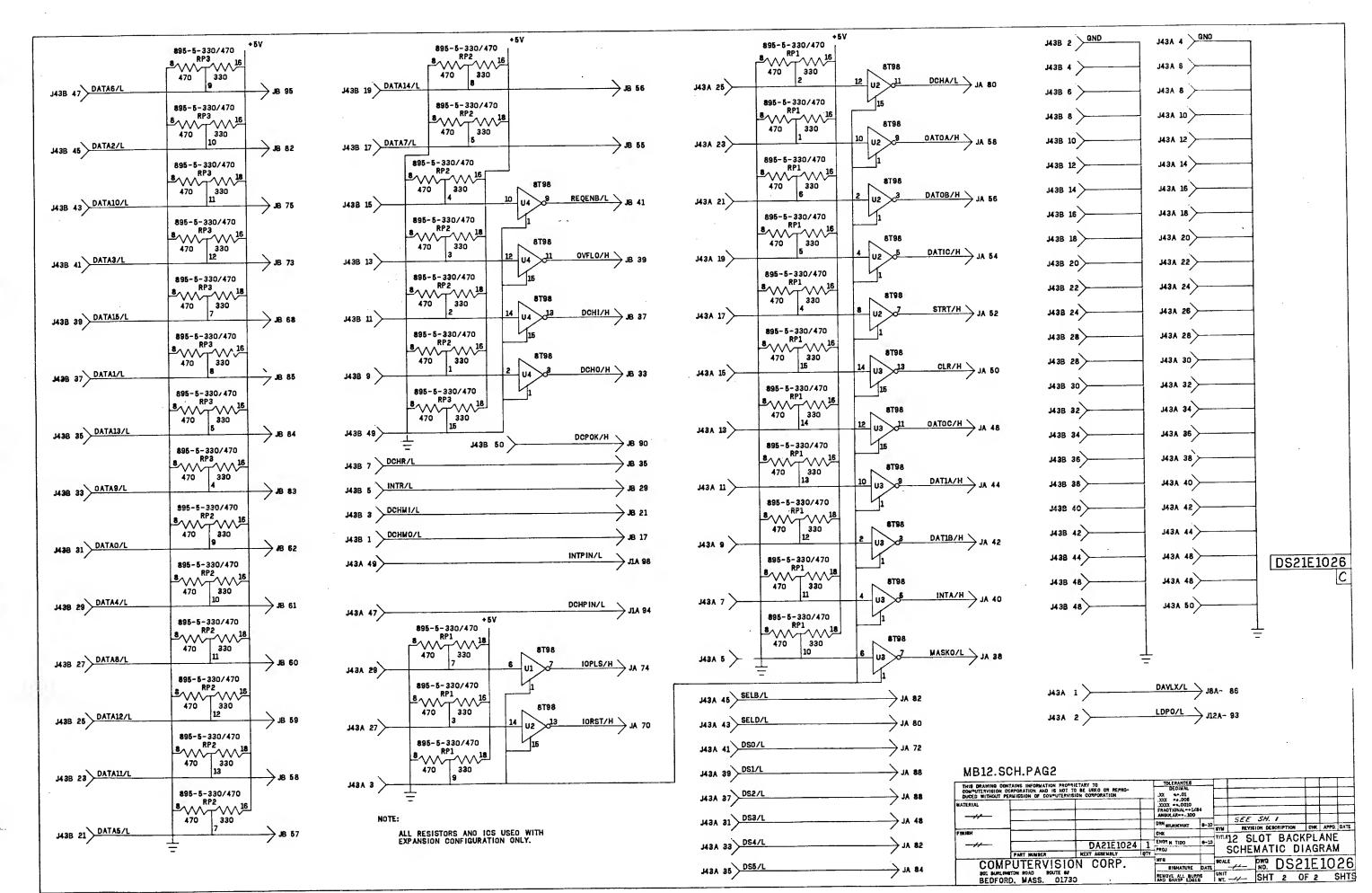
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### 12 Slot Backplane

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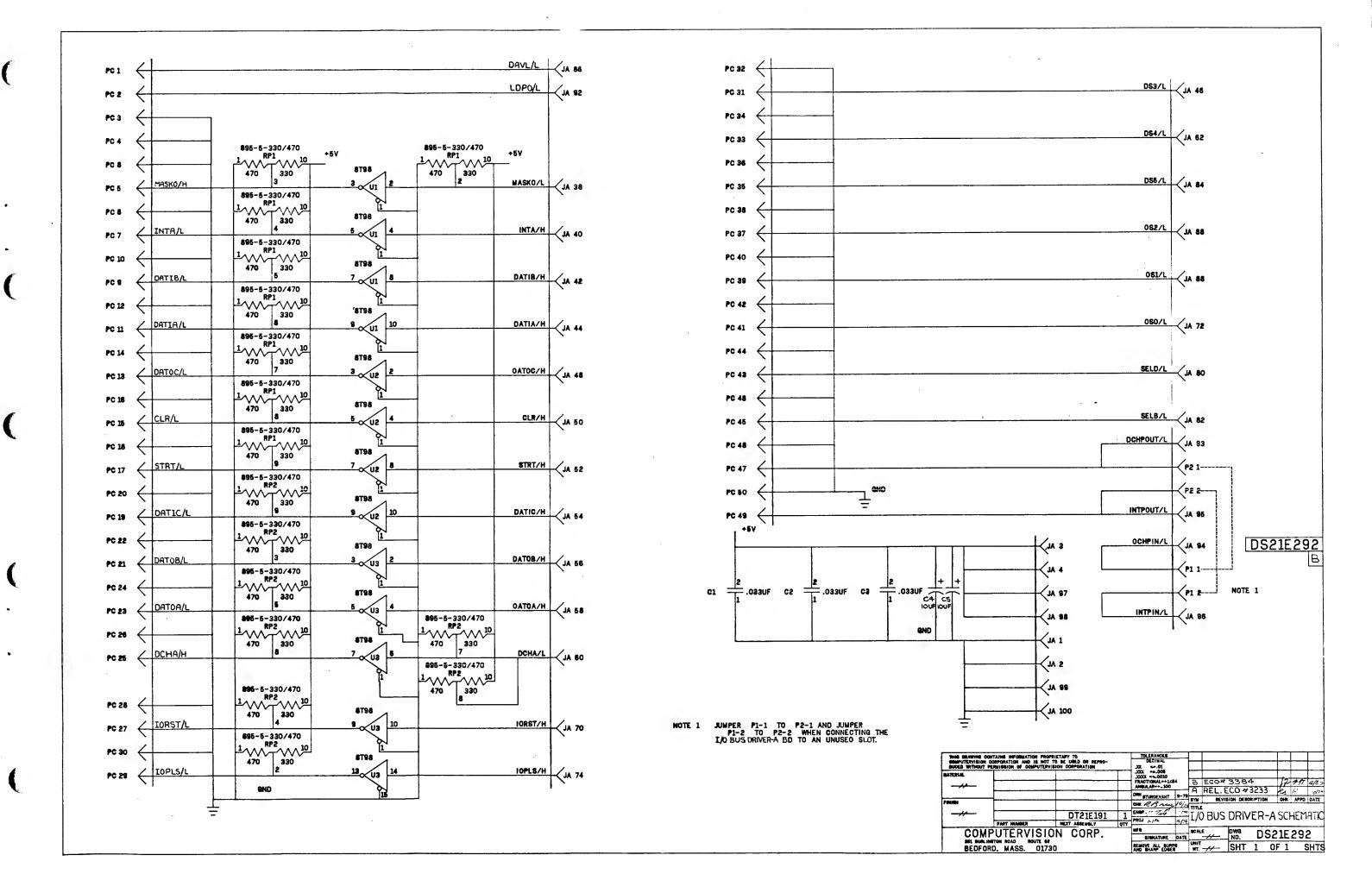


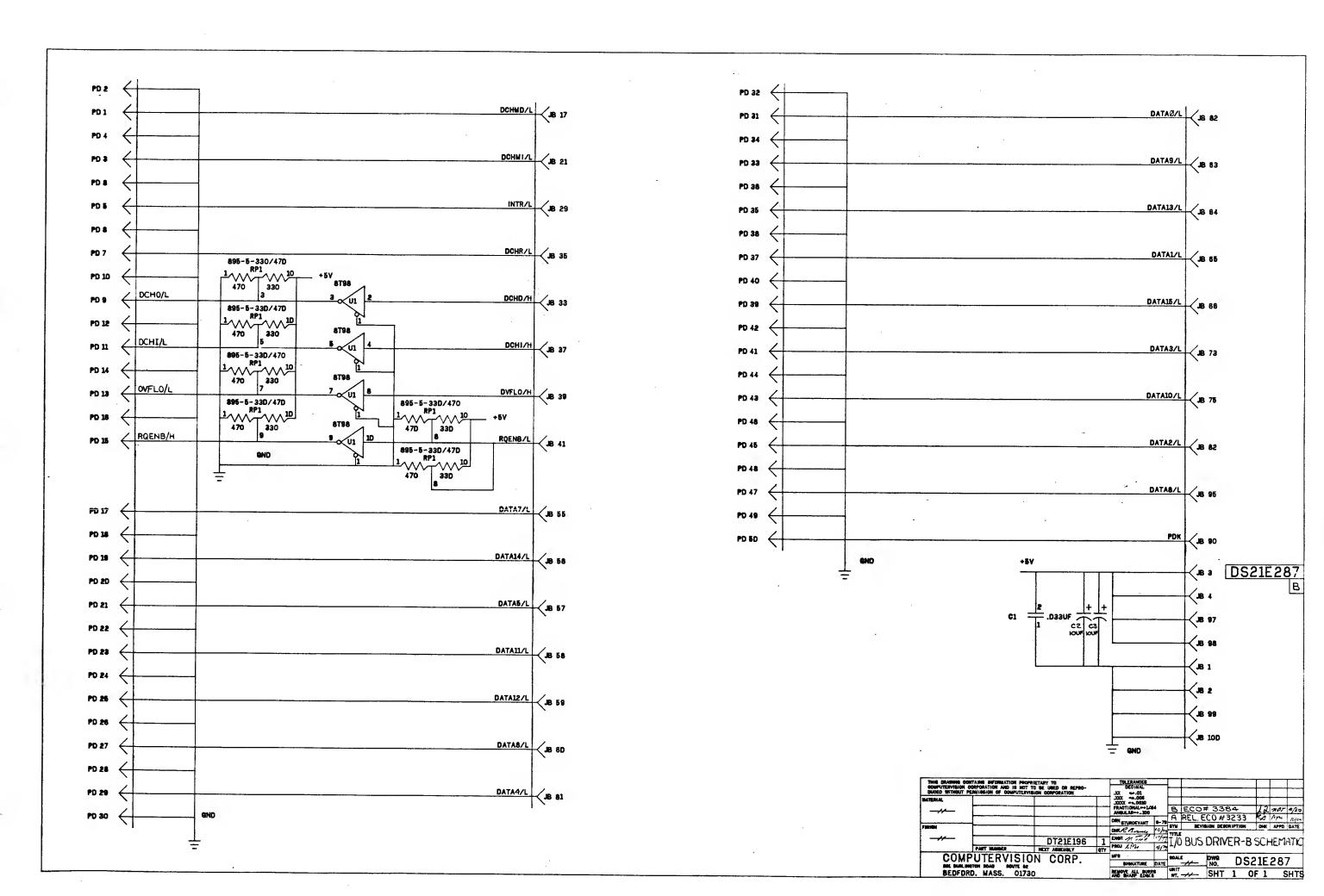
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### **Paddleboards**

A Schematic

B Schematic





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#### DA21E250-X CONFIGURATION TABLE

	SINGLE PORT	DUAL PORT. DISTRIBUTEO MODE	DUAL PORT. QPU MODE	SINGLE PORT ろこK
POPULATED WITH 4K RAMS (MK 4027-3)	USE CONFIGURATION BLOCKS A,A1,B	USE CONFIGURATION BLOCKS A.ALC.D.E	USE CONFIGURATION BLOCKS A.C.D.E	
POPULATED WITH 18K RAMS (MK 4116-3)	DA21E250-02 USE CONFIGURATION BLOCKS B.F	OA21E250-01 USE CONFIGURATION BLOCKS O.E.F.G	OA21E250-01 USE CONFIGURATION BLOCKS E.F.H	DA21E250-03 USE CONFIGURATION BLOCKS ALI

#### CONFIGURATION BLOCK A) 32K HARDWARE CONFIGURATION (USING 4K RAMS)

- 1) REMOVE R22
- 2) ADJUST POT R3/ SUCH THAT TP HAS A 29 JS REP RATE
  3) INSERT JUMPERS: JP9-2 . JP11-2 . JP13-2
  4) POPULATE MEMORY ARRAY WITH MK4027-3 MEMORY CHIPS

#### CONFIGURATION BLOCK ALL APORT 32K ADDRESSING CHART

* APORT FIELD	AMCO	AMC1	AMC2	AMC3	**CLOSED CONTACTS ON SWITCH PACK 1V
0	Н	Н	Н	Н	8
1	н	н	Н	L	7.8
2	н	н	L	Н	6.8
3	н	н	L	L	8.7.8
4	Н	L	Н	Н	5.8
5	Н	L	Н	L	5.7.8
6	Н	L	L	Н	5.8.6
7	н	L	L	L	5.8.7.8
8	L	н	н	Н	4.8
9	L	н	Н	L	4.7.8
10	L	Н	L	н	4 . 6 . 8
11	L	Н	L	L	4 .6 .7 .8
12	L	L	Н	Н	4 .5 .6
1.3	L	L	Н	L	4.5.7.6
14	L	L	L	Н	4.5.8.8
15	L	L	L	L	4.5.6.7.8

- \* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
- \*\* ALL DTHER CONTACTS ON SWITCH PACK IV OPEN

CONFIGURATION BLOCK B) SINGLEPORT CONFIGURATION i) DEPOPULATE PC BOARO AS PER BM21E250-02 2) ADD JUMPERS JP3 . JP5 . JP7

CONFIGURATION BLOCK C) BPORT 32K MEMORY ROW SELECT 1) INSERT JUMPERS: JP10-2 . JP12-2 . JP14-2

CONFIGURATION BLOCK D) BPORT 32K ADDRESSING AND 1/O DEVICE CODE CHART

*BPDRT FIELD	BMCO	BMCI	BMC2	BMC3	
OR	OR	OR	OR	OR	**CLOSED CONTACTS
I/O DEVICE CODE	BDSO	BOS1	BDS2	BDS3	ON SWITCH PACK 12S
0	Н	н	Н	Н	6
1	Н	н	Н	L	4.6
2 .	н	н	L	Н	3.6
2	H	н	L	L	3.4.8
4	Н	L	Н	Н	2.6
5	Н	L	н	L	2.4.6
6	Н	L	L	Н	2.3.6
7	Н	L	L	L	2.3.4.6
8	L	н	Н	Н	1.8
9	L	Н	Н	L	1.4.6
10	L	н	L	Н	1.3.6
11	L	Н	L	L	1.3.4.6
12	L	L	Н	Н	1.2.6
13	L	L	Н	L	1.2.4.8
14	L	L	L	Н	1.2.3.8
15	L	L	L	L	1.2.3.4.8

- \* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
- \*\* ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C OPEN

#### CONFIGURATION BLOCK E) LAST BDARD IN DAISY CHAIN

THE LAST DUAL PORT MEMORY BOARD IN A DAISY CHAIN MUST TERMINATE BPORT BUS SIGNALS. THE LAST DUAL PORT MEMORY IN A DAISY CHAIN ONLY MUST HAVE THE FOLLOWING RESISTORS: RPS.RP7.RPS. RP12 . RES PACK 12F

CONFIGURATION BLOCK F) 128K HAROWARE CONFIGURATION/APORT 128K ACCRESSING M

- 2) INSERT JIMPER JP4
  3) ADJUST POT R31 SUCH THAT TP HAS A 14.5 JJS REP RATE
  4) INSERT JUMPERS JP6 . JP11 . JP13
  6) POPULATE MEMORY ARRAY WITH MK4116-3 MEMORY CHIPS
- 8) APORT 128K ADDRESSING CHART

*APORT FIELD ND.	AMCO	ĀMC1	AMC2	AMC3	AMC3	**CLOSEO CONTACTS ON SWITCH PACK 1V
D.1.2.3	Н	Н	Н	Н	н	
4,5,8,7	н	н	Н	н	L	5
8,9,10,11	н	н	Н	L	Н	4
12.13.14.15	н	н	н	L	L	4.5
16.17.18.16	н	н	L	н	Н	3
2D.21.22.23	н	н	L	н	L	3.5
24.25.28.27	Н	н	L	L	н	3.4
28,28,30,31	н	Н	L	L	L	3.4.5
32.33.34.35	н	L	Н	Н	н	2
36.37.36.36	Н	L	Н	Н	L	2.5
40.41.42.43	Н	L	Н	L	Н	2.4
44.45.48.47	Н	L	н	L	L	2.4.5
46.46.50.51	Н	L	L	н	н	2.3
52.53.54.55	Н	L	L	н	L	2.3.5
58,57,56,56	н	L	L	L	Н	2.3.4
60.61.62.83	н	L	L	L	L	2.3.4.5
84.65.86.67	L	н	н	н	Н	1
68.69.7D.71	L	Н	н	Н	L	1.5
72,73,74,75	L	н	Н	L	Н	1.4
78.77.78.78	L	Н	Н	L	L	1 .4 .5
80.81.82.63	L	н	L	н	н	1.3
84.85.86.87	L	н	L	н	L	1.3.5
66,89,90,91	L	н	L	L	н	1.3.4
92,93,94,95	L	Н	L	L	L	1.3.4.5
98.97.98.99	L	L	н	Н	н	1.2
100,101,102,103	L	L	н	н	L	1.2.5
104,105,106,107	L	L	Н	L	н	1.2.4
106.106.110.111	L	L	Н	L	L	1 . 2 . 4 . 5
112.113.114.115	L	L	L	Н	Н	1 .2 .3
116.117.118.116	L	L	L	н	L	1.2.3.5
120.121.122.123	L	L	L	L	н	1.2.3.4
124,125,126,127	L	L	L	L	L	1.2.3.4.5

- \* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY (TO EXPANO BEYOND 15 FIELDS . IC 2X AND 2Y . SHT.7 . MUST BE ADDED)
- \*\* ALL OTHER SWITCH CONTACTS ON SWITCH IV ARE OPEN

CONFIGURATION BLDCK Q) 128K APDRT/32K BPORT COMMON MEMORY WITH JUMPERS JP10. JP12. JP14. INSERTED

BMC2	BMC3	COMMON SEGMENT OF APORT 128K MEMORY
Н	Н	15T 32K
н	L	2ND 32K
L	Н	3RD 32K
L	L	4TH 32K

2) TO FORCE COMMON APORT/BPORT MEMDRY INDEPENDENT OF BMC2 AND BMC3

BMC2	висз	COMMON SEGMENT OF APORT 126K MEMORY	JUMPERS INSERTED
X	X	1ST 32K	JP10. JP15. JP16
X	X	2ND 32K	JP1D. JP16
X	X	3RD 32K	JP10. JP15
X	Х	4TH 32K	JP10

WHERE X = DONT CARE

CONFIGURATION BLOCK H) BPORT 128K ADDRESSING CONFIGURATION

- 1) INSERT JUMPERS JP10. JP12. JP14
- 2) BPORT 128K ADDRESSING CHART

BPDRT FIELD NO.	BMADO	BMAD1	BMAD2	BMCO	BMC1	**CLOSED ON SWITC	CONTACTS
			1			9C	128
0.1.2.3	н	н	Н	н	н		8
4.5.8.7	н	Н	н	Н	L		2.6
6.9.10.11	н	н	н	L	н		1.8
12.13.14.15	н	н	н	L	L		1.2.8
16,17,16,16	н	н	L	н	н	7	6
20,21,22,23	н	н	L	н	L	7	2.6
24.25.28.27	Н	н	L	L	н	7	1.6
28,26,30,31	н	Н	L	L	L	7	1.2.8
32.33.34.35	н	L	н	Н	н	6	6
38.37.38.36	н	L	Н	Н	L	6	2.8
40.41.42.43	н	L	н	L	Н	8	1.8
44.45.46.47	Н	L	н	L	L	6	1.2.6
48,46,50,51	Н	L	L	н	н	6.7	8
52.53.54.55	н	L	L	Н	L	8.7	2.6
58.57.56.56	н	L	L	L	Н	6.7	1.6
80.61.62.63	Н	L	L	L	L	8.7	1.2.8
84,85,66.67	L	Н	н	н	Н	6	6
88.66.70.71	L	н	Н	Н	L	6	2.8
72.73.74.75	L	Н	Н	L	н	6	1.8
76.77.78.79	L	н	Н	L	L	5	1.2.8
80.61.62.63	L	Н	L	Н	Н	5.7	8
84.65.66.87	L	н	L	н	L	5.7	2.6
88.66.60.61	L	н	L	L	н	5.7	1.8
92.63.64.65	L	н	L	L	L	5.7	1.2.8
96.97.66.66	L	L	н	Н	н	5.6	6
10D.1D1.102.103	L	L	Н	Н	L	5.8	2.6
104.1D5.106.107	L	L	Н	L	Н	5.6	1.6
108.108.110.111	L	L	н	L	L	6.8	1.2.6
112,113,114,115	L	L	L	н	н	5.8.7	6
116,117,116,116	L	L	L	н	L	5 .6 .7	2.8
120.121.122.123	L	L	L	L	н	5 .6 .7	1.6
124,125,128,127	1	L	L	L	L	5.6.7	1.2.8

EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY ALL OTHER CONTACTS ON SWITCH PACK 12S AND 8C OPEN (8C-2 May be closed to disable aport)

CONFIGURATION BLOCK 1) 32K SINGLE PORT CONFIGURATION (USING 18K RAMS)

1) DEPOPULATE BOARDS AS PER ASSEMBLY DA21E250-03

#### MISCELLANEOUS JUMPERS

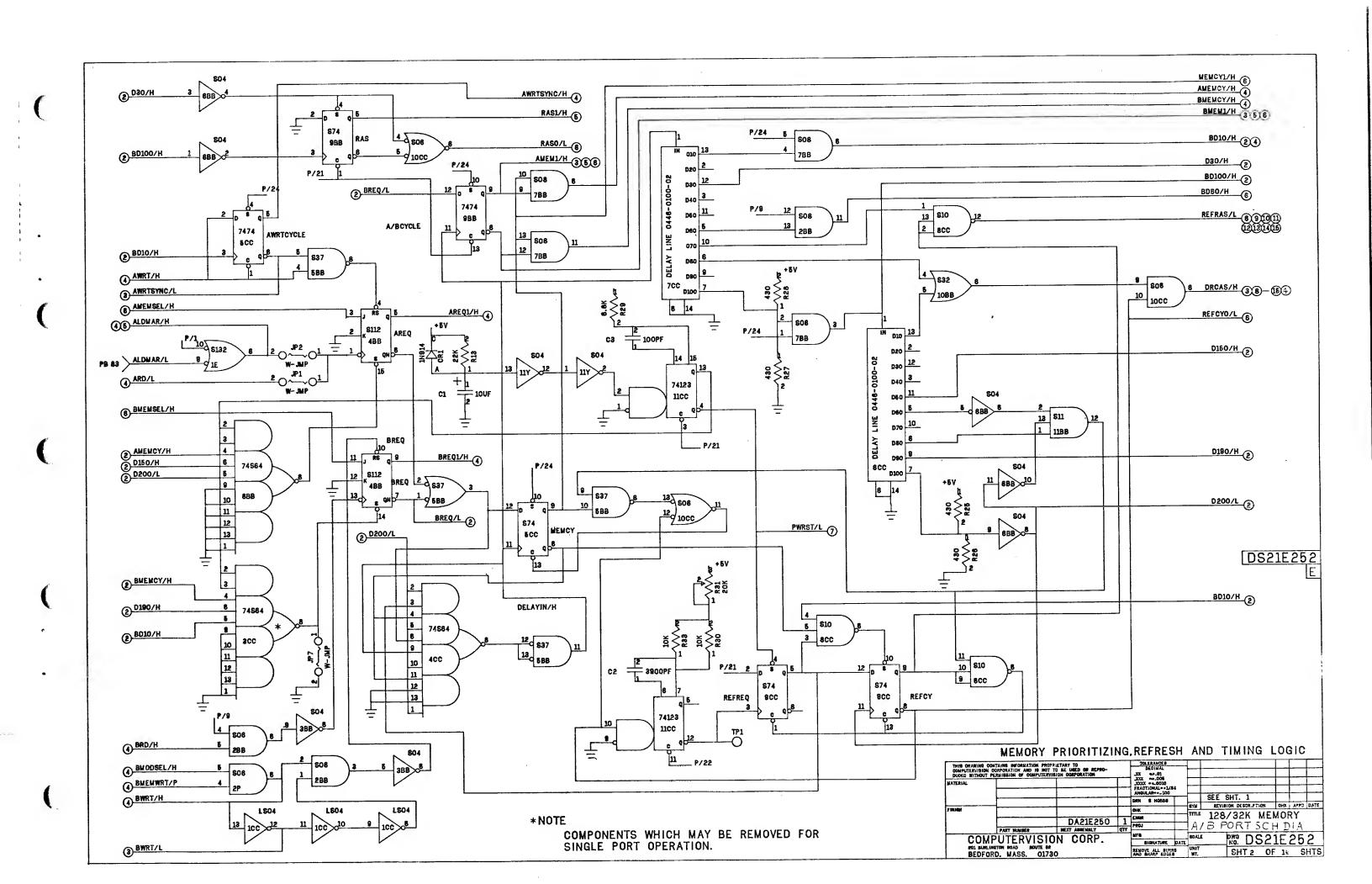
- 1) FOR LDMAR STARTING APORT MEMORY CYCLE INSERT JP-2 2) FOR MEMREAO STARTING APDRT MEMORY CYCLE INSERT JP-1 3) FOR GPU MODE REQUIRING DISABLED APORT . CLDSE SWITCH 8C-2
- 4) APORT MUC/NON MUC OPERATION

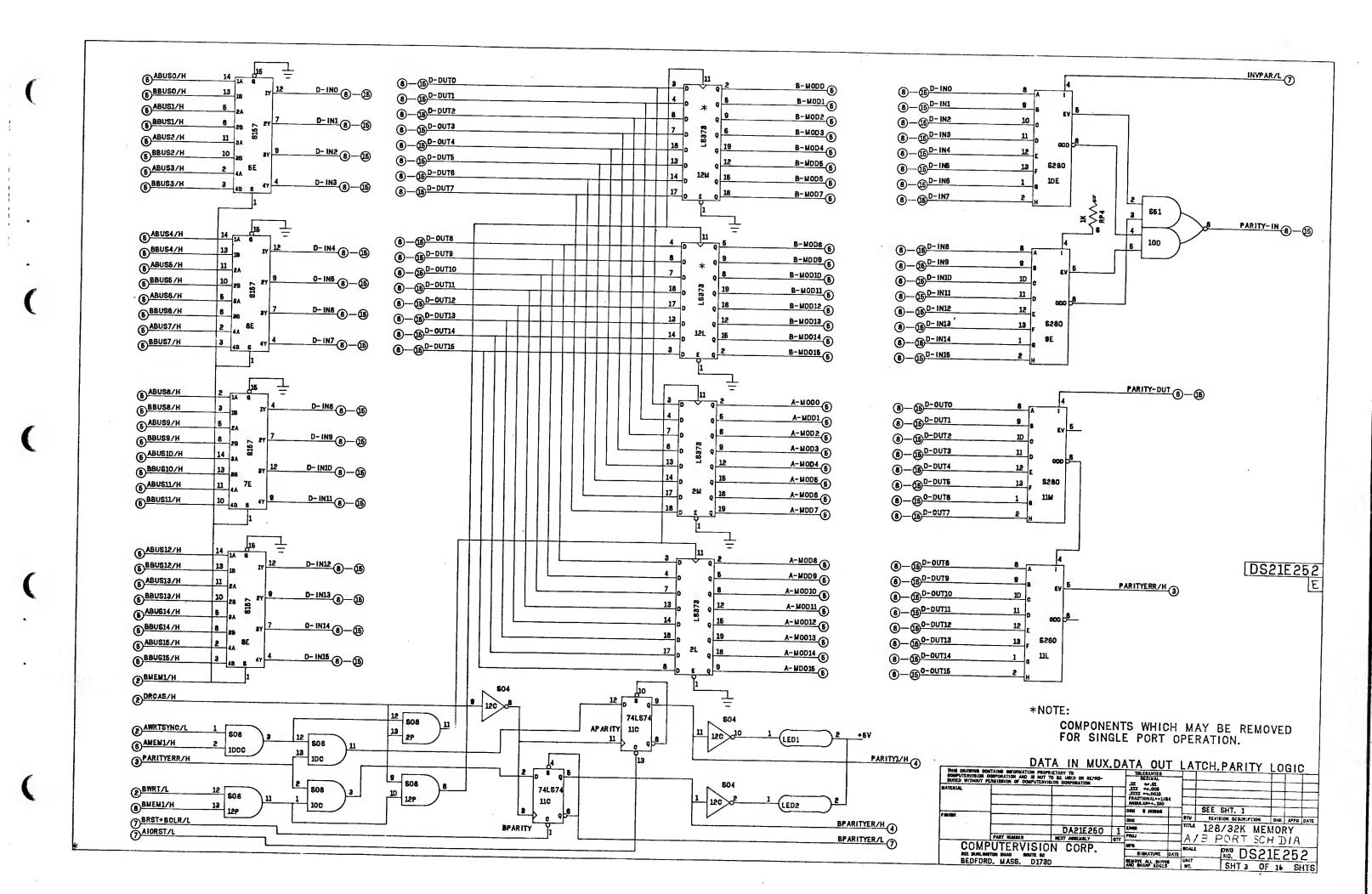
JUMPER PLUG 40	)
MUC OPERATION	1-18 2-15 3-14 4-13
NON MUC DPERATION	5-12 6-11 7-10 8-9

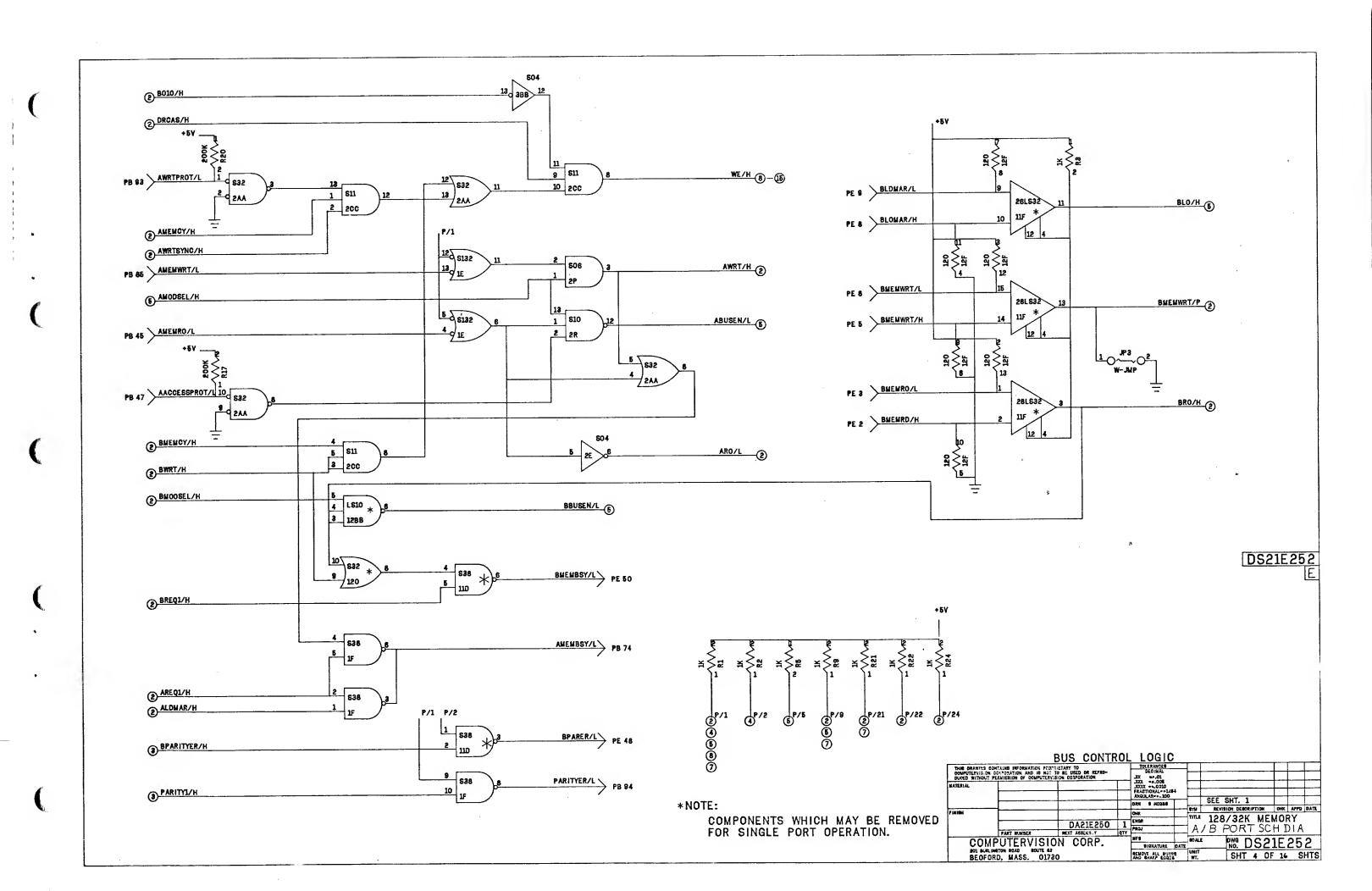
6) APORT I/O DEVICE CODE

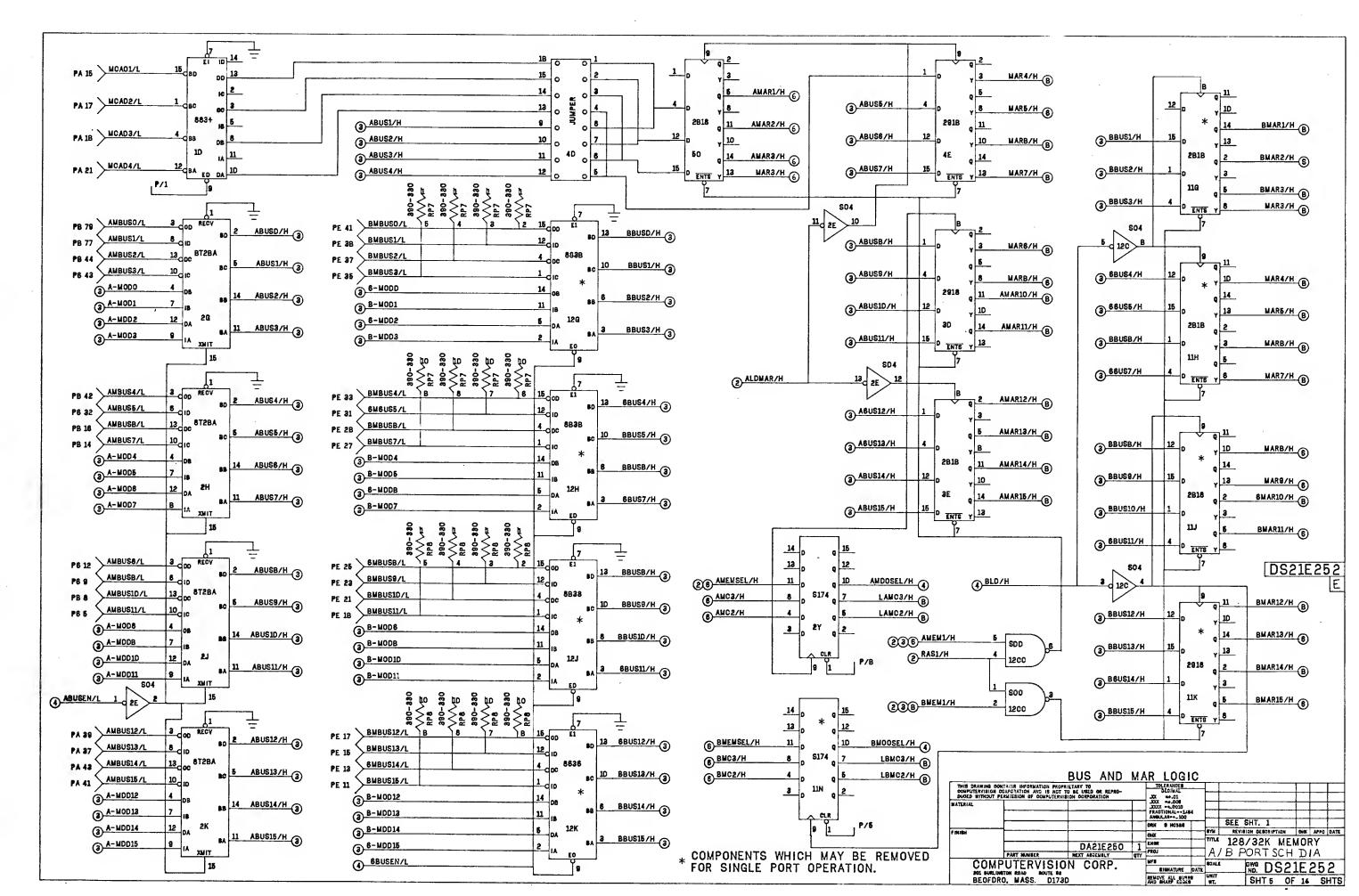
1) STANDARD 24g. INSERT JP8 FOR 25g

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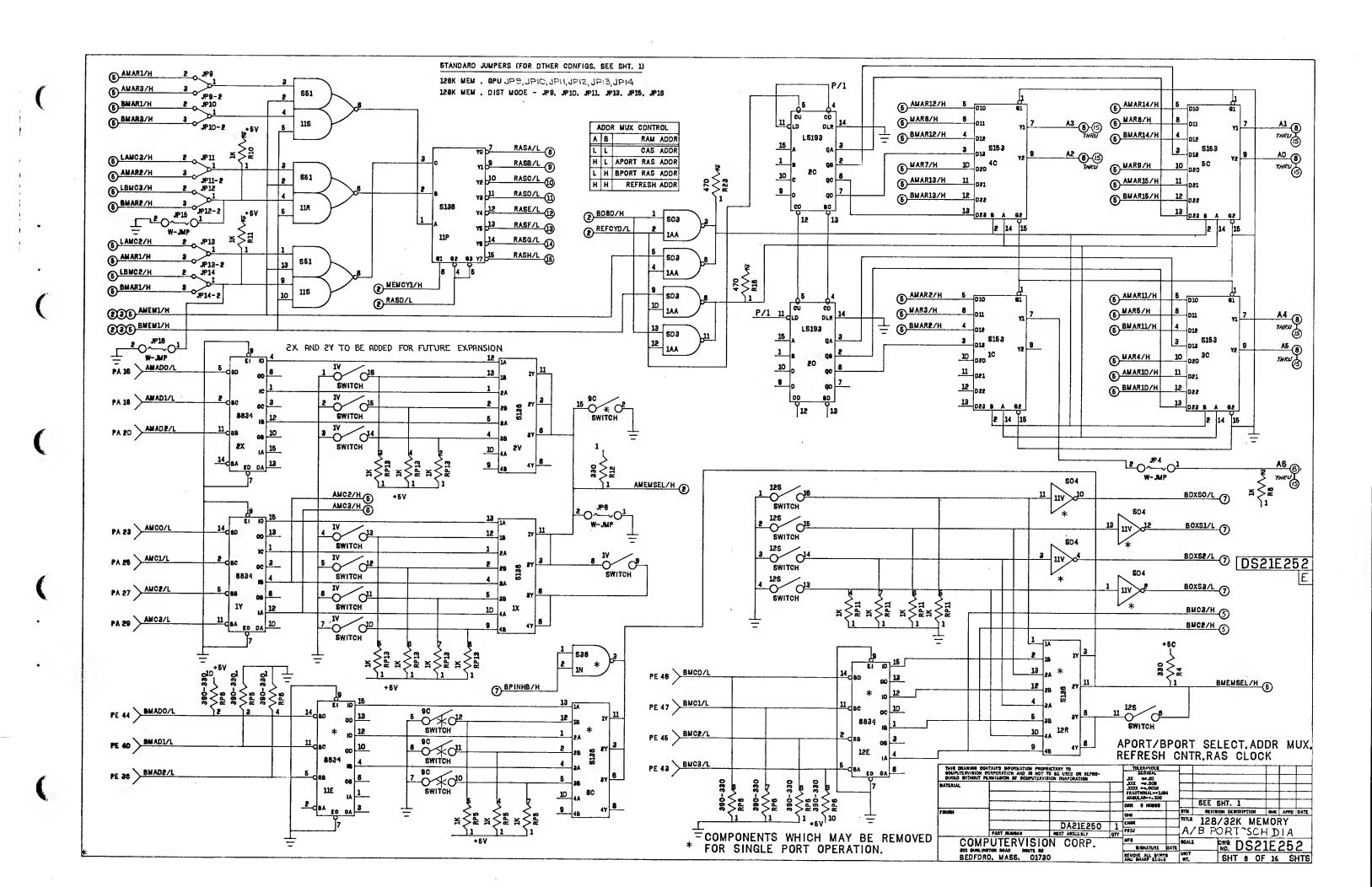


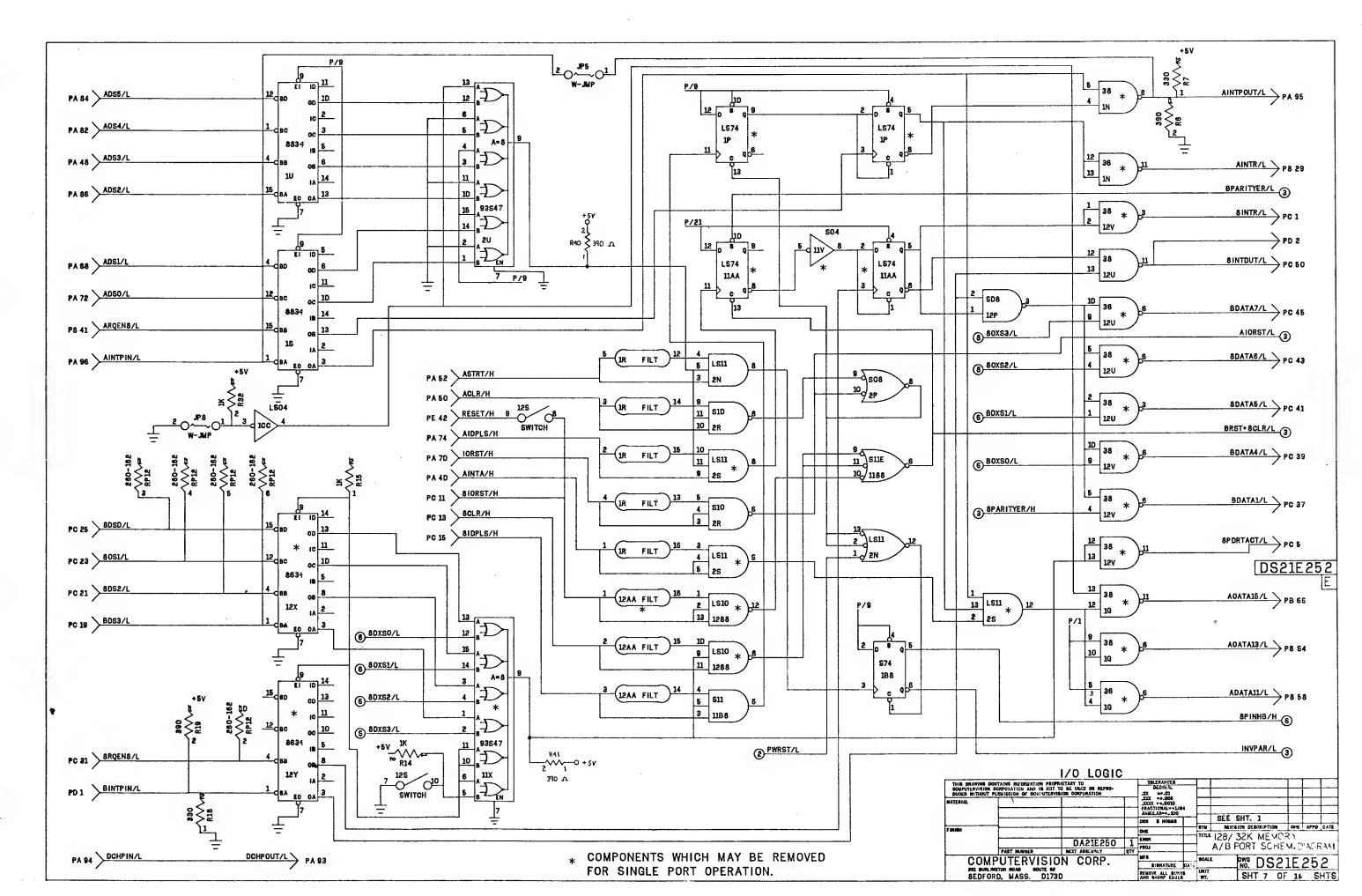


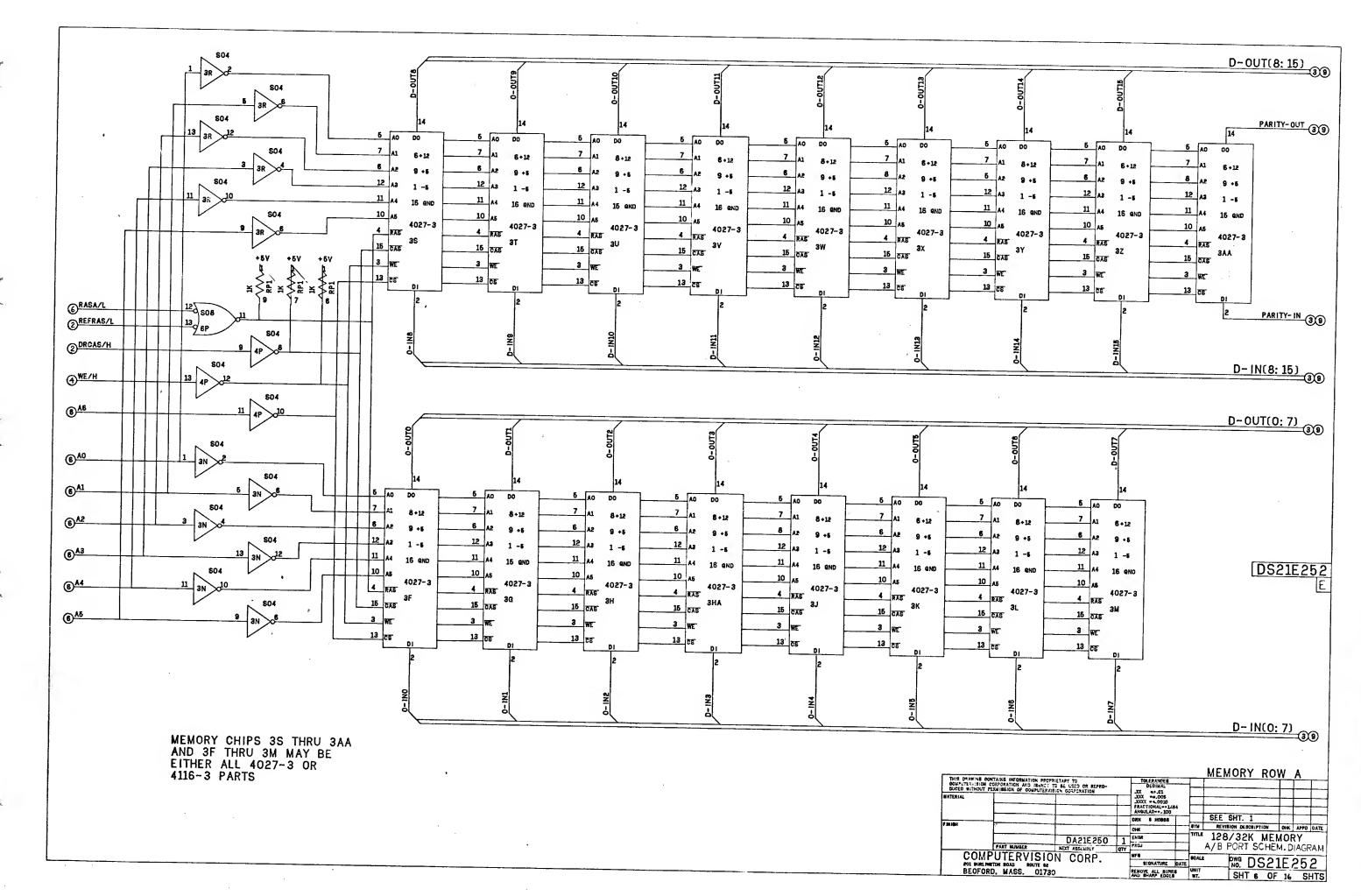


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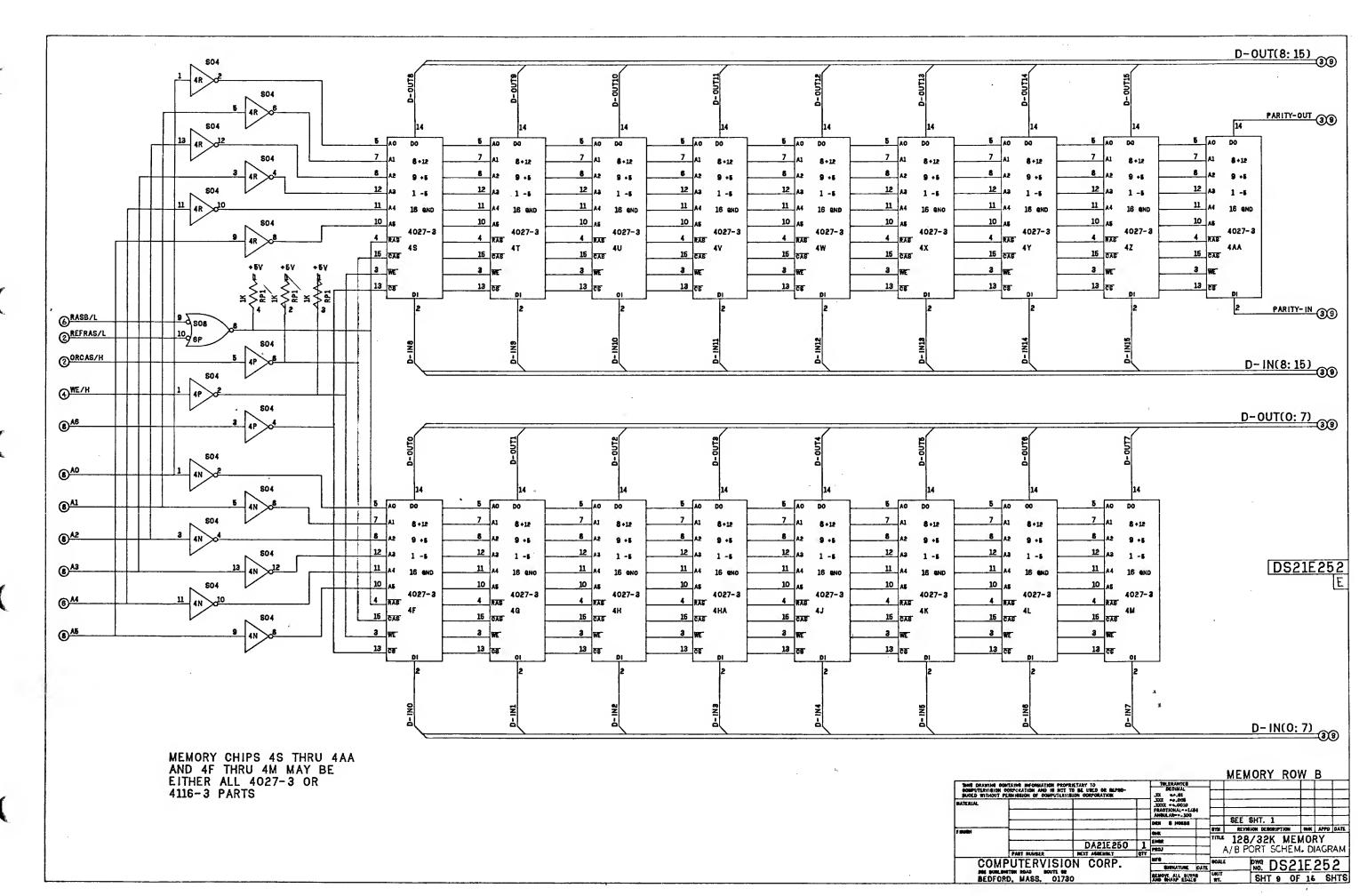


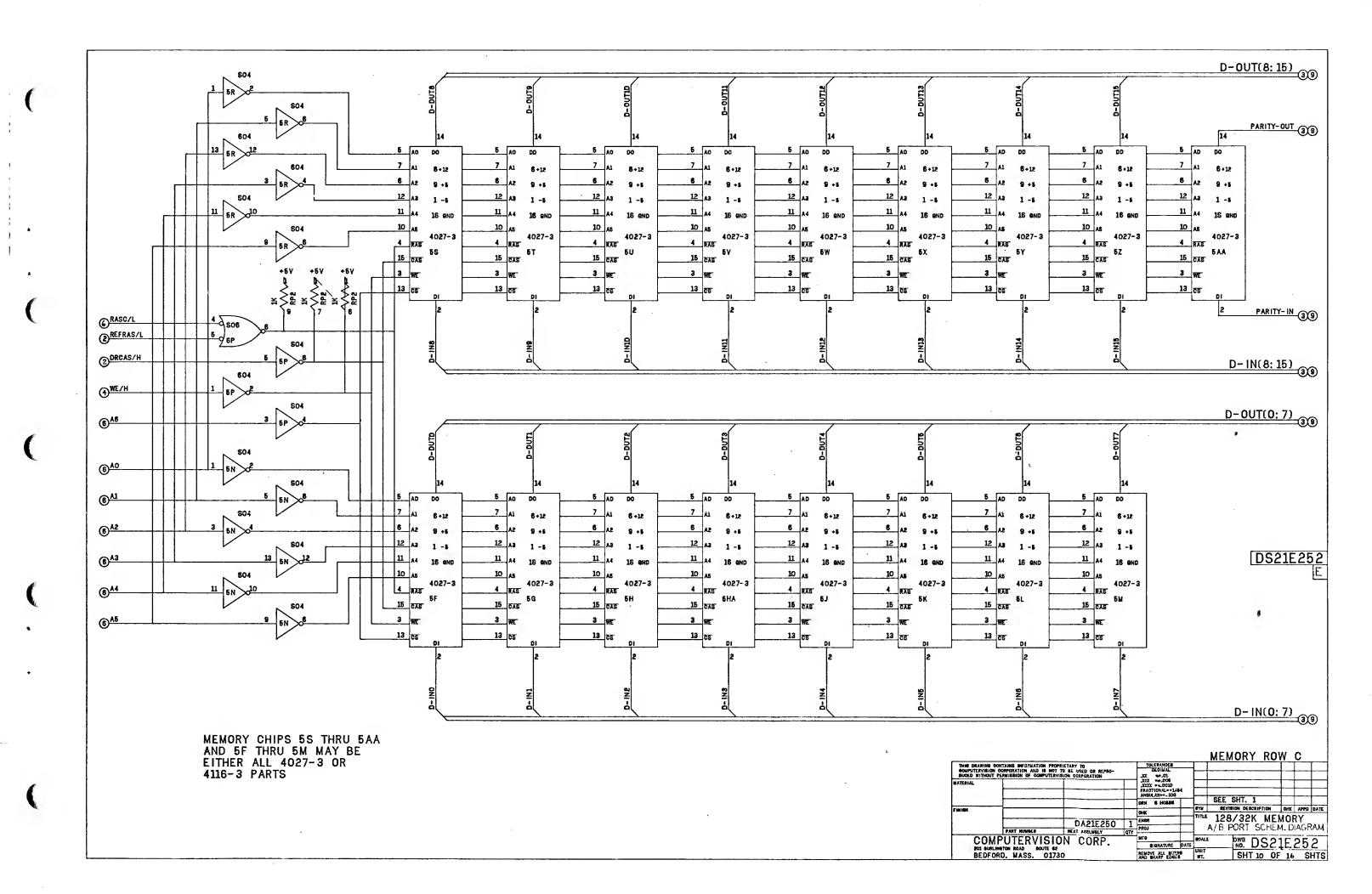


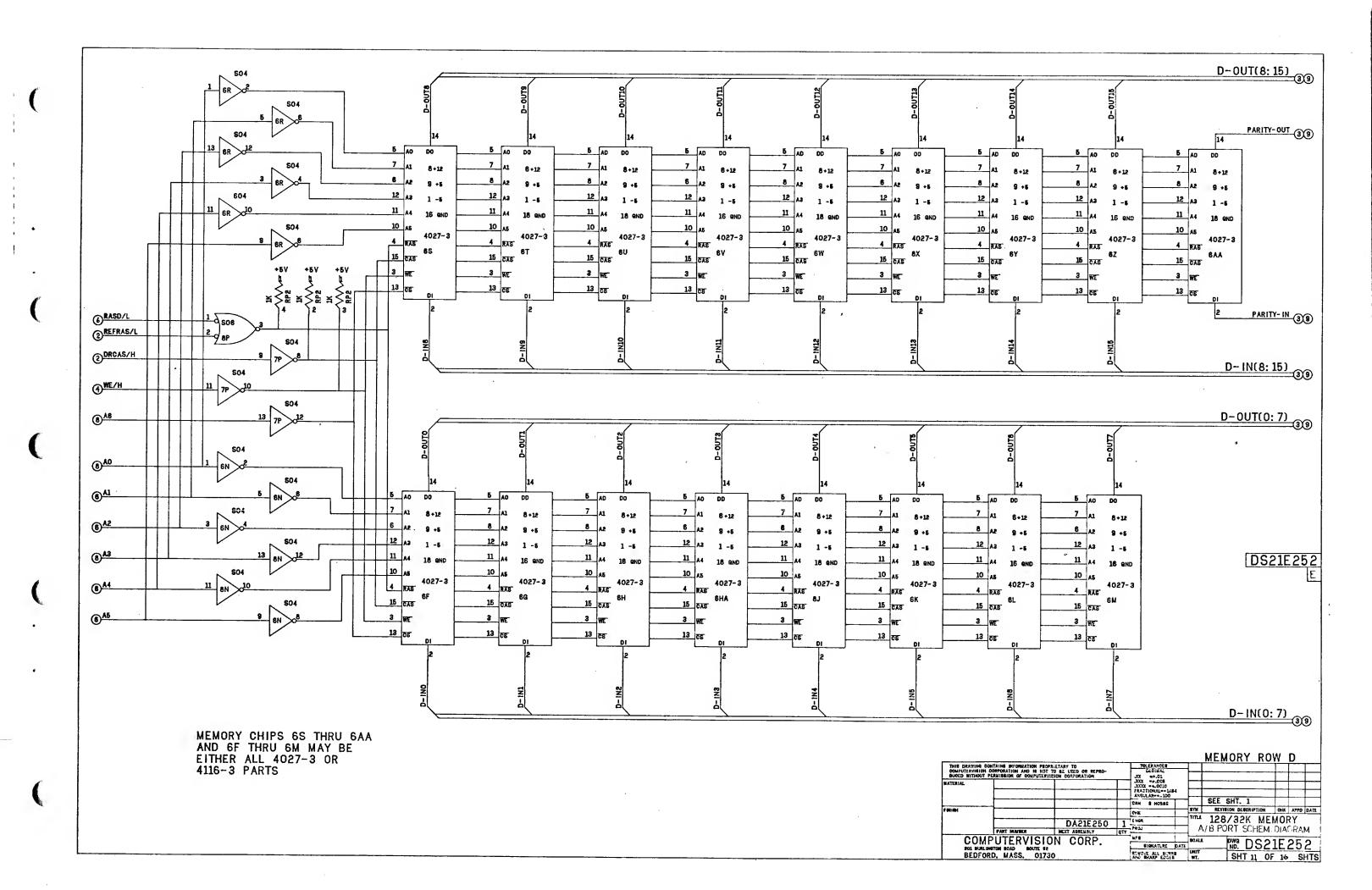


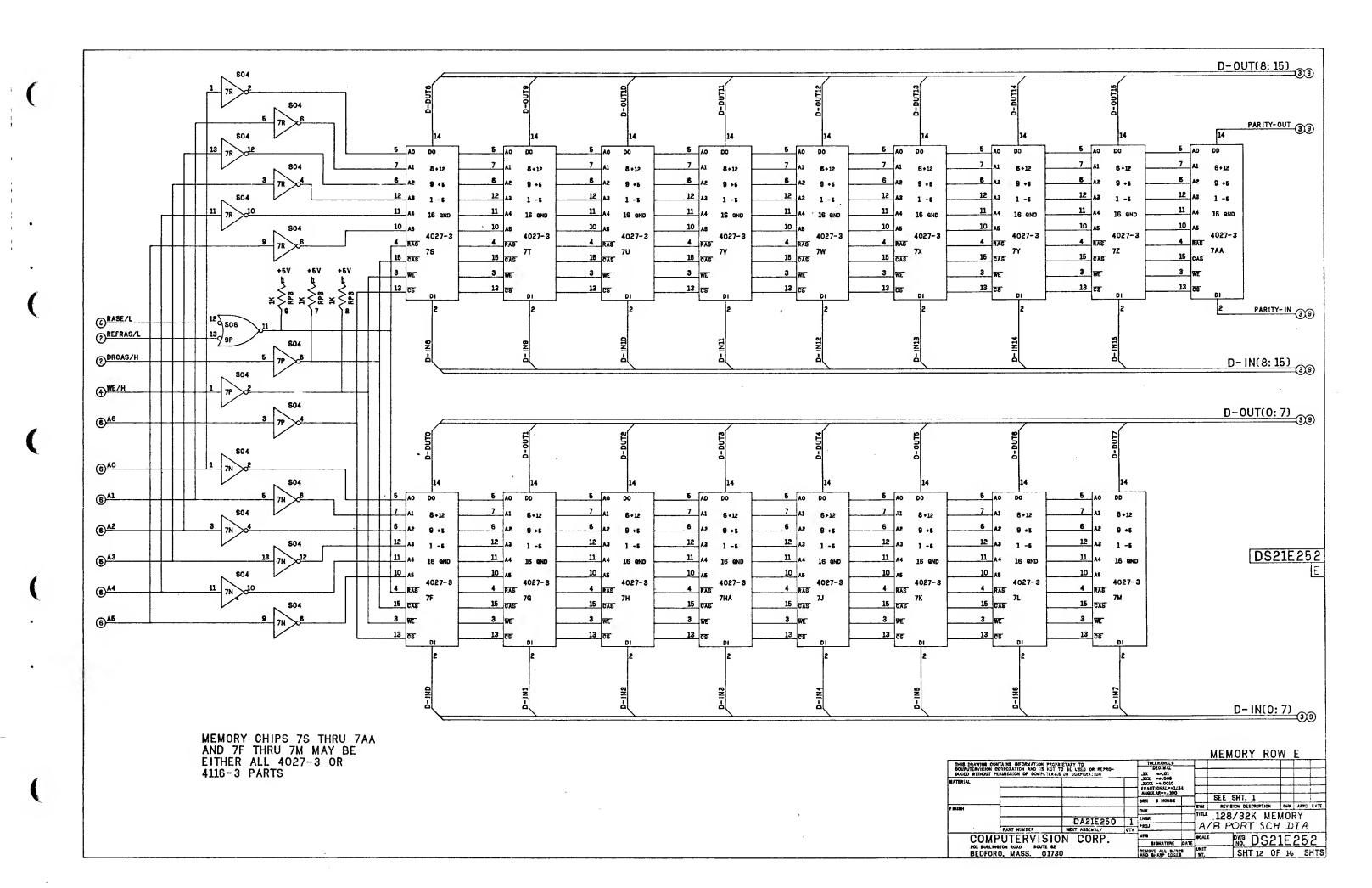
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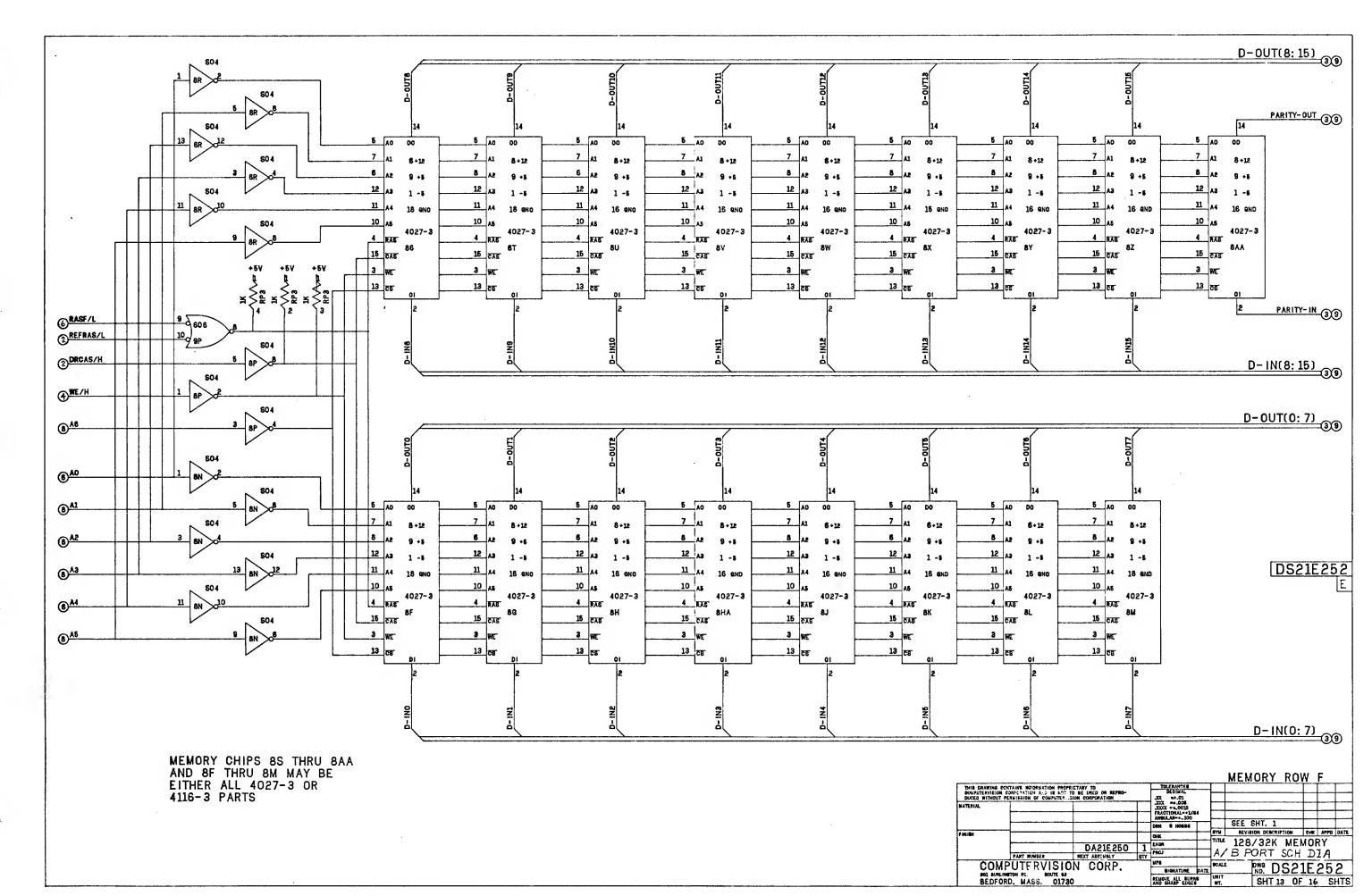
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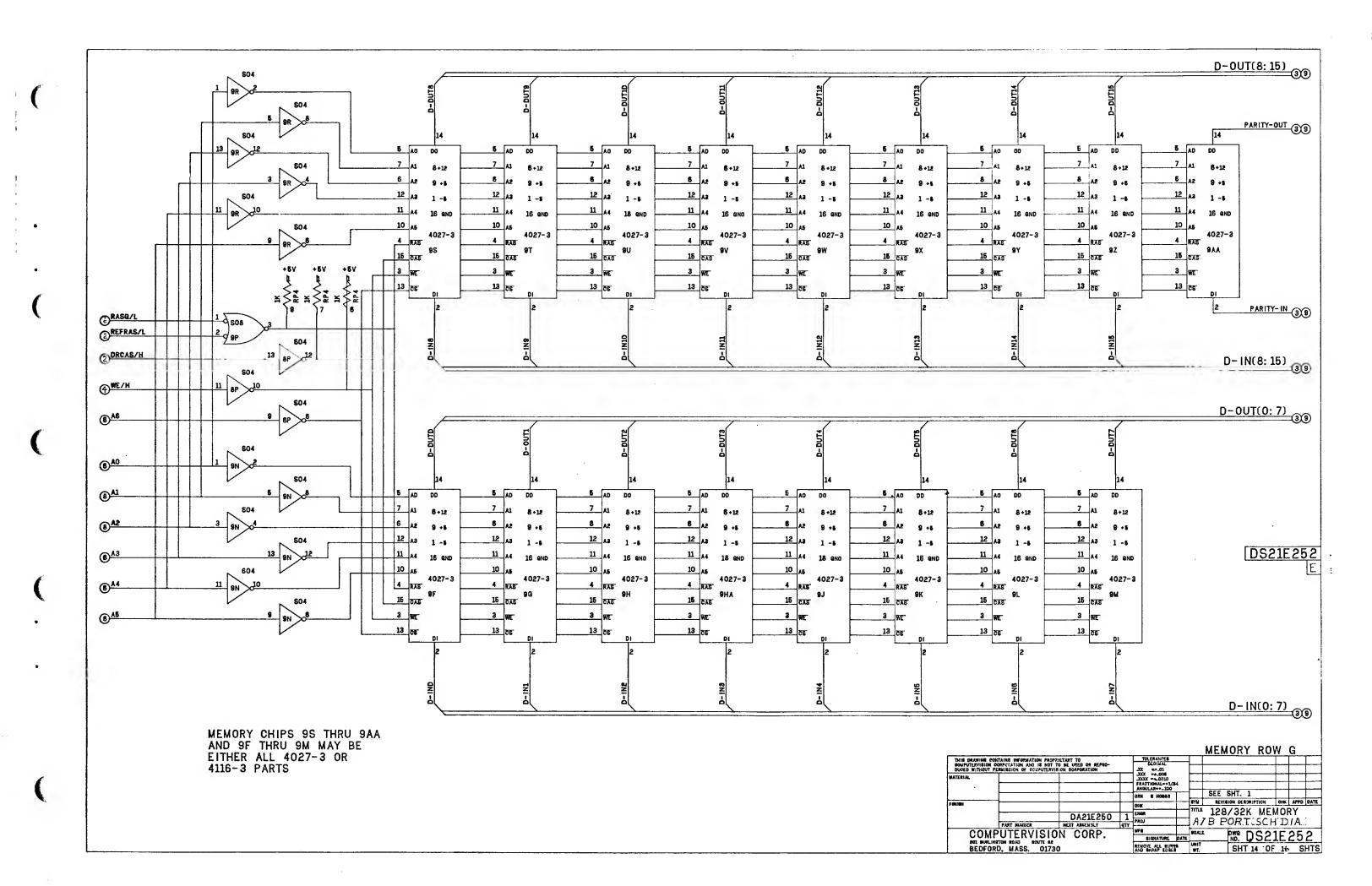


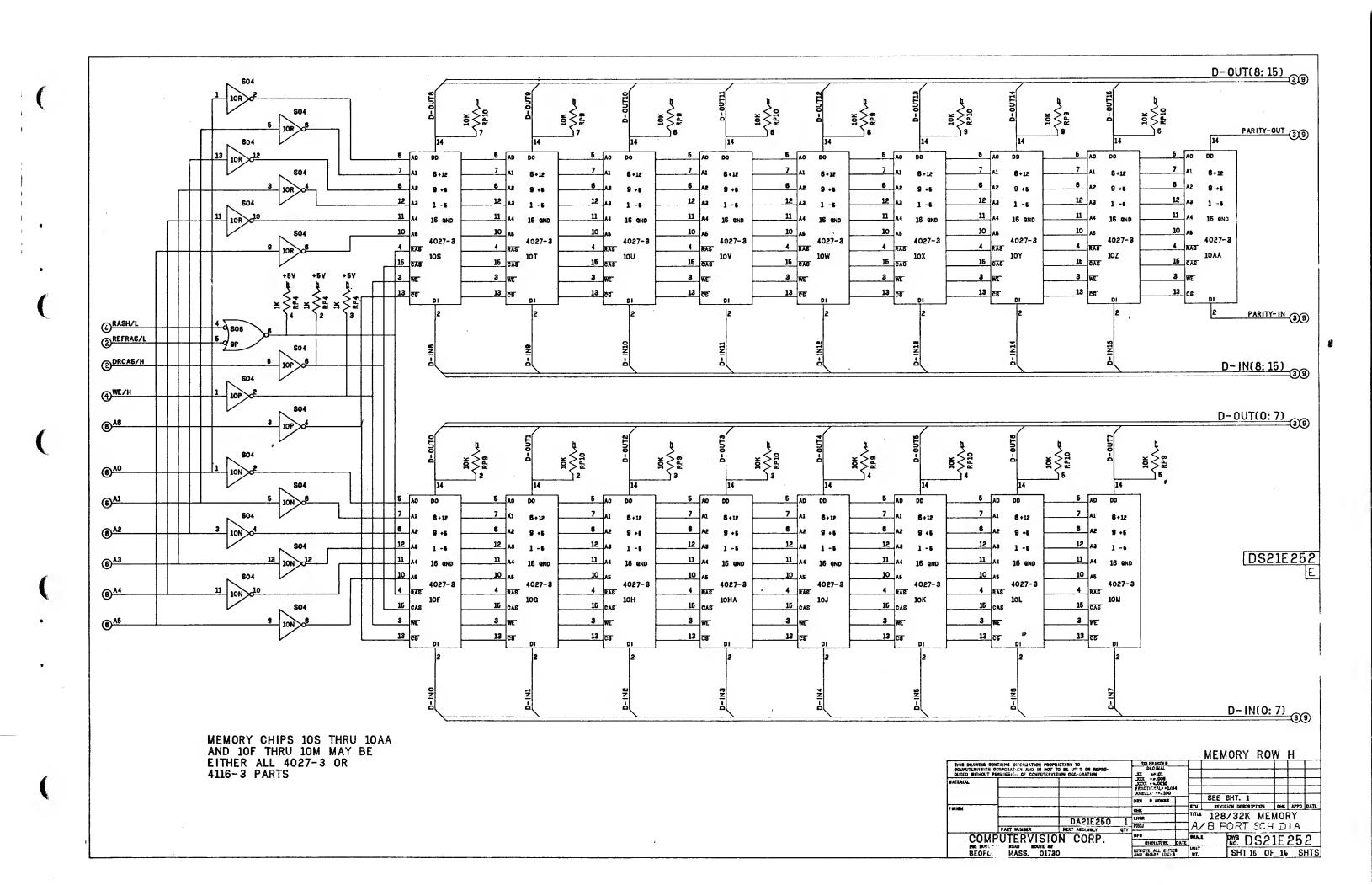


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#### B PORT CONNECTORS

CONN C

CONN E

BINTR		2
		4
BPORTACT		6
		8
		10
BIORST		12
BCLR		14
BIOPL6		16
		18
BDS 3		20
BDS 2		22
BDS 1		24
BDS 0		26
		28
		30
BRQENS		32
		34
BDATA 10		36
BOATA 1		38
BDATA 4		40
BDATA B		42
BDATA 8		44
BOATA 7		46
FREE		48
	BINTPOUT	50

1		B MEM RD	2
3	B MEM RO		4
5	B MEMWRT	BMEMWRT	8
7		BLDMAR	8
8	BLOMAR		10
11	B MEM BUS 15		12
13	B MEM BUS 14		14
15	B MEM BUS 13		16
17	B MEM BUS 12		18
19	B MEM BUS 11		20
21	B MEM BUS 10		22
23	B MEM BUS 9		24
25	B MEM BUS 8		26
27	B MEM BUS 7		28
29	B MEM BUS 6		30
31	B MEM BUS 5		32
33	B MEM BUS 4		34
35	B MEM BUS 3		36
37	B MEM BUS 2	BMY05	38
39	B MEM BUS 1	BWAD1	40
41	B MEM BUS O	RESET	42
43	BMC 3	BWADO	44
45	BMC 2	BVCO	46
47	BMC 1	BPARER	48
49		B MEM BUSY	50

ALL UNUSED PINS GROUNDED

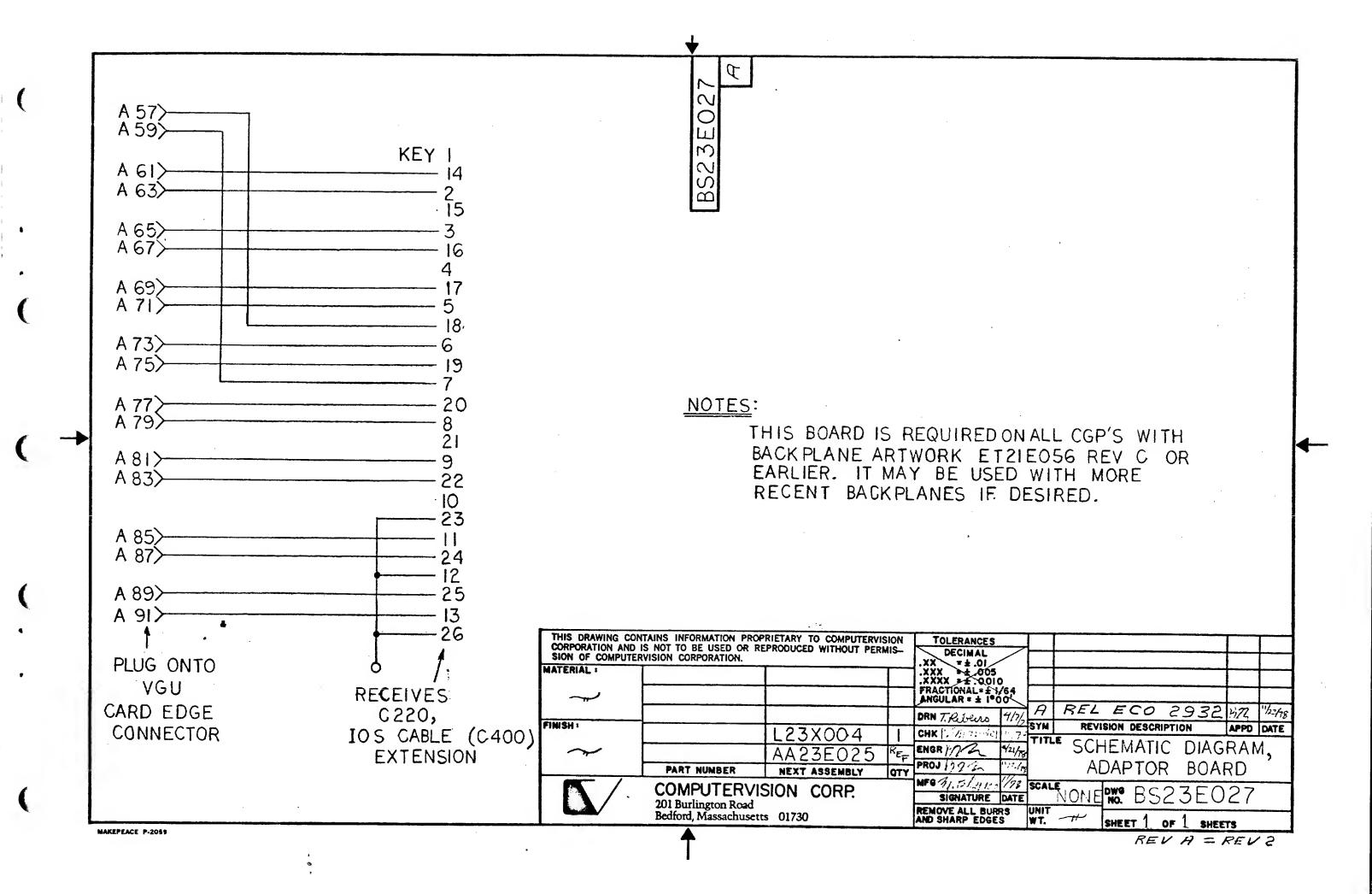
DS21E252

VOLTAGE FEED	S FOR CONNECTORS PA.PB
+12 VOLTS	B46.A7.A8
-5 VOLTS	B81
-12 VOLTS	B71.B72
+5 VOLTS	A/B3,A/B4,A/B97,A/B98
GNO	A/B1, A/B2, A/B99, A/B100

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## **VGU Adaptor Board**

Schematic



### REMARKS FORM

CHNICAL or EDITORIAL ERRORS (inc	
	clude page number):
CHNICAL or EDITORIAL ERRORS (inc	clude page number):
GGESTIONS FOR IMPROVEMENT:	
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